WE CLAIM:

1. A DRAM, comprising:

at least one primary sense amplifier, wherein the at least one primary sense amplifier has data storage and data write-back capability, and has at least two amplification stages; and

a single ended bitline structure, wherein a storage cell and the at least one primary sense amplifier are connected by a single bitline, wherein the DRAM has storage cells and bitlines.

2. The DRAM of claim 1, further comprising a single ended global bitline structure, wherein the at least one primary sense amplifier and a secondary sense amplifier are connected by a single global bitline, wherein the DRAM has secondary sense amplifiers and global bitlines.

3. The DRAM of claim 2, wherein the DRAM further comprises a small voltage swing design.

4. The DRAM of claim 2, wherein at least one of the secondary sense amplifiers comprise at least two amplification stages.

5. The DRAM of claim 2, wherein the at least one primary sense amplifier is being capable to decouple from the global bitline.

6. The DRAM of claim 1, wherein the at least one primary sense amplifier comprises MOS devices, and wherein at least one of the MOS devices has a customized threshold.

7. The DRAM of claim 6, wherein the customized threshold is dynamically adjusted.

8. The DRAM of claim 1, wherein the DRAM is an embedded DRAM.

9. A DRAM, comprising:

a single ended bitline structure, wherein the DRAM has bitlines;

a single ended global bitline structure, wherein the DRAM has global bitlines;

a plurality of primary sense amplifiers operationally engaging the bitlines and the global bitlines, wherein the primary sense amplifiers have data storage and data write-back capability, and wherein the primary sense amplifiers are being capable to decouple from the global bitlines;

a full-wordline I/O structure, wherein essentially all memory cell that are simultaneously turned on by any one wordline are being operated on by associated sense amplifiers of the primary sense amplifiers, wherein the DRAM has memory cells and wordlines; and

a pipelined architecture, wherein the DRAM is functioning in cycles and in each of the cycles an operation can be initiated, and wherein the pipelined architecture comprise synchronized operations of the single ended bitline structure, of the single ended global bitline structure, of the primary sense amplifiers, and of the full-wordline I/O structure.

10. The DRAM of claim 9, further comprising a reduced address space, wherein the reduced address space has no column address.

11. The DRAM of claim 9, wherein a Read command and a subsequent WriteBack command of the commands are executed in differing cycles of the cycles.

12. The DRAM of claim 9, wherein a Read command and a subsequent WriteBack command of the commands are executed in a single one of the cycles.

13. The DRAM of claim 9, wherein at least two of the commands are executed simultaneously in a single one of the cycles.

14. The DRAM of claim 13, wherein a Read command and a Write command of the commands are executed simultaneously in a single one of the cycles.

15. The DRAM of claim 9, wherein a size of the DRAM can be increased in a modular manner.

16. The DRAM of claim 15, wherein the modular manner increase comprise an I/O increase.

17. The DRAM of claim 15, wherein the modular manner increase comprise a banking increase.

18. The DRAM of claim 9, wherein the DRAM further comprises a small voltage swing design.

19. The DRAM of claim 9, wherein at least one of the plurality of primary sense amplifiers comprise at least two amplification stages.

20. The DRAM of claim 9, wherein the DRAM is an embedded DRAM.

21. A processor, comprising:

at least one embedded DRAM macro, wherein the at least one embedded DRAM macro is further comprising:

a single ended bitline structure, wherein the DRAM has bitlines;

a single ended global bitline structure, wherein the DRAM has global bitlines;

a plurality of primary sense amplifiers operationally engaging the bitlines and the global bitlines, wherein the primary sense amplifiers have data storage and data write-back capability, and wherein the primary sense amplifiers are being capable to decouple from the global bitlines;

a full-wordline I/O structure, wherein essentially all memory cell that are simultaneously turned on by any one wordline are being operated on by associated sense amplifiers of the primary sense amplifiers, wherein the DRAM has memory cells and wordlines; and

a pipelined architecture, wherein the DRAM is functioning in cycles and in each of the cycles an operation can be initiated, and wherein the pipelined architecture comprise synchronized operations of the single ended bitline structure, the single ended global bitline structure, the primary sense amplifiers, and the full-wordline I/O structure.

22. The processor of claim 21, wherein the DRAM further comprises a reduced address space, wherein the reduced address space has no column address.

23. The processor of claim 21, wherein the DRAM further comprises a small voltage swing design.